# Gradient Descent Bit-Flipping Algorithms for Fault-Tolerant Memories

Bane Vasic

Motivation: During the past four decades, the decrease in transistor size and the increase in integration factor have been the driving force for semiconductor memories, and have led to very small and fast memory chips. As the demands for higher memory capacity and read/write speed continue, it is widely recognized that a sustainable progress can be only achieved through highly energy-efficient transistors. The proposed research is concerned with developing advanced error correction schemes for fault-tolerant memories. Our approach is based on codes on graphs and iterative decoding. It attractiveness lays in the theoretical guarantee that the hardware overhead required to to ensure reliable operation grows only linearly with the memory size even when both memory elements as well as logic gates are faulty.

Objectives and Methodology: In this project we will consider a fault-tolerant bit flipping (BF) algorithm on the binary symmetric channel (BSC). The decoder we plan to develop is inspired by two decoders: Wadayama's Gradient Descent Bit Flipping (GDBF) [8] and Miladinovic and Fossorier's Probabilistic Bit Flipping (PBF) [9]. The GDBF was designed for the Additive White Gaussian Noise (AWGN) channel and shown to provide good balance between steady convergence and decoding speed.

Our approach is to introduce either deliberate errors as recently suggested by Sundararajan, Winstead, and Boutillon [4] and in [3]) or faulty-hardware-induced in variable node processors as a means of improving the GDBF. We will combine this with the property of PBF where code bits with a number of unsatisfied check sums larger than a fixed threshold are flipped with some probability, which is adapted throughout the iterations. By combining the ideas of [8] and [9] with some critical improvements following from our intuition on fault-tolerant decoders, we will design a hard decision decoder, resilient to logic gate failures.

We will answer a bold hypothesis whether probabilistic behavior of a decoder due to unreliable components can be exploited to our advantage and lead to an improved performance and reduced hardware redundancy. This seemingly counterintuitive idea is motivated by our recent insights in iterative decoding dynamics: as iterative decoding can be viewed as a recursive procedure for Bethe free energy function minimization, randomness in a message update helps the decoder to escape from local minima. Our recent results [3] strongly suggest that such decoding behavior may be possible.

Contribution to France-US Scientific Collaboration: In addition to technical contributions, this project will greatly contribute to continuing the fruitful collaboration between the University of Cergy Pontoise and University of Arizona, which includes (i) the dual degree graduate program, between the two institutions, (ii) research activities on the FET-program project (i-RISC) and (iii) Fulbright scholar grant which is devoted to establishing closer research ties among researchers from US, France and Serbia. As part of this activities two postdoctoral researchers (from France and Serbia), and have visited University of Arizona in 2014 and 2014, Dr. Vasic has taught at the European School of Information Theory in 2013, and Prof. Declercq visited the University of Arizona for a full year.

References

[1] T. Wadayama, K. Nakamura, M. Yagita, Y. Funahashi, S. Usami, and I. Takumi, "Gradient Descent Bit Flipping algorithms for decoding LDPC codes," IEEE Transactions on Communications, vol. 58, no. 6, pp. 1610–1614, June 2010.

[2] N. Miladinovic and M. Fossorier, "Improved Bit-Flipping decoding of low-density parity-check codes," IEEE Trans. Inform. Theory, vol. 51, no. 4, pp. 1594–1606, April 2005.

[3] O.-A. Rasheed, P. and Ivanis, B. Vasic, "Fault-Tolerant Probabilistic Gradient-Descent Bit Flipping Decoders," *IEEE Commun. Letters*, vol. 18, no. 9, pp. 1487 - 1490, September 2014.

[4] G. Sundararajan, C. Winstead, and E. Boutillon, "Noisy Gradient Descent Bit-Flip Decoding for LDPC Codes," 2014. [Online]. Available: http://arxiv.org/abs/1402.2773.