PROF. DR. BANE VASIC

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INVITED BY

ETIS LABORATORY
RESEARCH LABORATORY IN INFORMATION PROCESSING AND SYSTEMS

Dr. Bane Vasic is a Professor of Electrical and Computer Engineering and Mathematics at the University of Arizona. He is affiliated with BIO5, the Institute for Collaborative Beoresearch, and is a Director of the Error Correction Laboratory.

Dr. Vasic is an inventor of the soft error-event decoding algorithm, and the key architect of a detector/decoder for Bell Labs magnetic recording read channel chips which were regarded as the best in industry. Different variants of this algorithm were implemented in virtually all magnetic hard drives. His pioneering work on structured low-density parity check (LDPC) error correcting codes and invention of codes has enabled low-complexity iterative decoder implementations. Structured LDPC codes are today adopted in a number of communications standards and in extremely high-density magnetic storage systems.

Dr. Vasic is known for his theoretical work in error correction coding theory and codes on graphs which has led to analytical characterization of the hard decision iterative decoders of LDPC codes, and design of codes with best error-floor performance known today.

He is an IEEE Fellow and da Vinci Fellow.

CURRENT RESEARCH INTERESTS

- Error Correction Coding Theory, Information Theory, Theoretical Biology, Coding and Detection for Information Storage, Coding and Modulation for Optical Communications.

EDUCATION

- 1994:   Ph.D. in Electrical Engineering, University of Nis, Serbia.

  The youngest Doctor at University of Nis, School of Engineering.
- 1991:   MS in Electrical Engineering, University of Nis, Serbia.
- 1989:   Dipl.-Ing. in Electrical Engineering, University of Nis, Serbia.

  Award for student with the largest GPA at the University.

  One of three scholarship holders of Serbian Academy of Science and Arts from the University of Nis.

PUBLICATIONS

- [Publication list](#)