

Curriculum Vitæ et Studiorum

Salvatore Monteleone

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Contacts

Name Surname and title Salvatore Monteleone, PhD

Date of birth December 24, 1985

City of birth Siracusa, Italy

Status Married

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Google Scholar Profile <https://scholar.google.com/citations?user=bvwZ0EEAAAAJ>

Current and Past Positions

11/2019 – current Research Fellow within the Fellows-in-Residence program at CY Advanced Studies and ETIS Lab (UMR 8051 CNRS), ENSEA, CY Cergy Paris University (formerly University of Cergy-Pontoise), Cergy-Pontoise, France.

09/2015 – 10/2019 Adjunct Professor, Department of Electrical, Electronics, and Computer Engineering, Università degli Studi di Catania, Catania, Italy

05/2014 – 04/2019 Research Assistant, Department of Electrical, Electronics, and Computer Engineering, Università degli Studi di Catania, Catania, Italy

Education

- Jan 30, 2014 Ph.D. Degree in Computer & Communication Engineering.
University of Catania, Italy.
Dissertation entitled “Security and Privacy Policy Management in Dynamic and Context-aware User-centric Systems”.
- Apr 22, 2010 M.Sc. degree in Computer Engineering, (grade 110/110 cum laude).
University of Catania, Italy.
- Oct 11, 2007 B.Sc. degree in Computer Engineering, (grade 110/110).
University of Catania, Italy.

Qualifications

- 07/2010 Qualification to practice the profession of Engineer in Italy.
Order of Engineers of the Province of Catania.
Engineer Section A, Sector C (IT Engineering).
- 07/2007 Certification “Safety and hygiene at work” (120h course).
Knowledge of safety and health prescriptions to be implemented in the workplace (Italian Legislative Decree 626/94) and in temporary or mobile construction sites (Legislative Decree 494/96).
Faculty of Engineering, University of Catania, Italy.

Work in projects

- 11/2019 – today Research on “Design Methodologies for Energy Efficient Emerging NoC Architectures” within the Fellows-in-Residence program.
CY Advanced Studies and ETIS Lab (UMR 8051 of the CNRS), ENSEA, CY Cergy Paris Université, France.
- 08/2018 – 10/2019 Research on “Techniques and methodologies for multi-objective optimization of parametric within the M9 project” M9 development contract project (CDS 000448) - CUP: C32F18000100008.
Department of Electrical, Electronic, and Computer Engineering (DIEEI), University of Catania, Catania, Italy.
- 05/2018 – 04/2019 Research on ubiquitous and pervasive systems within the MISE project - HORIZON 2020 - PON 2014/2020 “SUMMIT – Multi-platform support for IoT applications” (PROG. N. F / 050270 / 01-03 / X32).
Department of Electrical, Electronic, and Computer Engineering (DIEEI), University of Catania, Catania, Italy.
- 11/2015 – 05/2018 Research on ubiquitous and pervasive systems within the PON project “SERVIFY - SERVIce FirstlY” (PON03PE_00132_1).
Department of Electrical, Electronic, and Computer Engineering (DIEEI), University of Catania, Catania, Italy.

- 05/2014 – 10/2015 Research on ubiquitous and pervasive systems within the PON 2007-2013 project “SMART HEALTH - CLUSTER OSDH - SMART FSE - STAYWELL” (PON04a2_C).
Department of Electrical, Electronic, and Computer Engineering (DIEEI), University of Catania, Catania, Italy.
- 02/2014 – 03/2014 Technical support for experimental development within the PO FESR 2007-2013 project "RammaR - Programmable cybernetic system of verbal interaction interfaces" (CUP G63F11000530004).
Definition and implementation of a leap tracking system integrated into a Spoken Dialog System.
Department of Electrical, Electronic, and Computer Engineering (DIEEI), University of Catania, Catania, Italy.
- 12/2010 – 04/2014 Definition of architectural specifications and development within the European project FP7-ICT-2009-5 called "Webinos - Secure WebOs Application Delivery Environment" (Grant Agreement n.257103 - CUP E67G10000060006). Definition of the architecture (based on PrimeLife and XACML) for the management of security and protection of privacy in the webinos system. Subsequent implementation of the designed components.
Department of Electrical, Electronic, and Computer Engineering (DIEEI), University of Catania, Catania, Italy.
- 07/2010 – 11/2010 Study, implementation and testing of APIs and Policy Manager (of XACML-based policy) for the BONDI framework of WAC. Porting of the code implemented by Symbian to Android and to Unix based systems, “Mobile Web, applications and services based on Web technologies on mobile terminals” project.
Department of Computer and Telecommunications Engineering (DIIT), Faculty of Engineering, University of Catania, Catania, Italy.

Teaching

The teaching portfolio includes computer architectures, cloud computing, and programming with JavaScript.

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| Academic Year
2019/20 | Lecturer of the “Hardware Accelerators for DNNs” module (12h) Ph.D. Course of “Engineering for the Innovation” University of Palermo, Palermo, Italy. |
| Academic Years
2018/19
2017/18
2016/17
2015/16 | Adjunct Professor in “Computer Architectures” (9 C.F.U.), Degree Course in Electronic Engineering, Department of Electrical, Electronic, and Computer Engineering (DIEEI), University of Catania, Catania, Italy. |
| Academic Year
2017/18 | Adjunct Professor in “Cloud Computing” (40h), Master “Empowering Knowledge Intensive Business Services (KIBS): Innovatori/Imprenditori Specializzati in KIBS”, University of Palermo, Palermo, Italy. |

Academic Year 2014/15	Lecturer of “JavaScript Lab.” (18h), Degree Course in Computer Engineering, Department of Electrical, Electronic, and Computer Engineering (DIEEI), University of Catania, Catania, Italy.
Academic Years 2017/18 2016/17 2014/15	Lecturer of “Architectures for Fixed and Mobile Systems Lab.”, Degree Course in Computer Engineering, Department of Electrical, Electronic, and Computer Engineering (DIEEI), University of Catania, Catania, Italy.

Memberships

- ACM Member
- HiPEAC affiliate member
- IEEE Senior Member: #91287102 - Italy Section
- IEEE Internet of Things Community Member
- IEEE Sustainable ICT Community Member
- IEEE Young Professionals Member

Seminars

Jan 28, 2020	“The Network-on-Chip paradigm: Challenges and Opportunities”, Seminar to Fellows @ MIR, CY Cergy Paris Université.
Jan 23, 2020	“Design Methodologies for Energy Efficient Emerging NoC Architectures (E3NoC)”, ETIS Lab, ENSEA
Oct. 7, 2018	Tutorial: Simulation of Networks-on-Chip with Noxim, <i>2018 IEEE International Conference on Computer Design (ICCD)</i> .
Jul. 4, 2014	“Secure Smart Objects and Mobile Services: La sicurezza end-to-end per gli Smart Objects”. “ <i>Small Devices - Big Data: sicurezza in un mondo senza fili</i> ”, Università degli Studi di Roma “La Sapienza”.

Research area of interest

Embedded systems design & applications with contributions mainly focused on low-power design, Network-on-Chip architectures, and Cyber-Physical Systems (CPS).

Services to the Research Community

Positions as Chair

NoCArc 2020 <i>TPC Chair</i> <i>Web Chair</i>	13 th International Workshop on Network on Chip Architectures (NoCArc’20). Held in conjunction with the 53 rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-53), October 18, 2020, Athens, Greece. Will be held virtually during the week of the conference.
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CF 2020 <i>Publicity Chair</i> <i>Local Chair</i> <i>Session Chair</i>	17 th ACM International Conference on Computing Frontiers 2020 (CF'20). May 11-13, 2020, Catania, Italy. Held virtually during the week of the conference.
NoCArc 2019 <i>TPC Chair</i> <i>Web Chair</i>	12 th International Workshop on Network on Chip Architectures (NoCArc'19). Held in conjunction with the 52 nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-52), October 13, 2019, Columbus, Ohio, USA.
NoCArc 2018 <i>Web Chair</i>	11 th International Workshop on Network on Chip Architectures (NoCArc'18). Held in conjunction with the 51 st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-51), October 20, 2018, Fukuoka City, Japan.
PEC 2018 <i>Session Chair</i>	3 rd International Conference on Pervasive and Embedded Computing, part of PECCS, the 8th International Joint Conference on Pervasive and Embedded Computing and Communication Systems, July 29-30, 2018, Porto, Portugal.
NoCArc 2017 <i>Web Chair</i>	10 th International Workshop on Network on Chip Architectures (NoCArc'17). Held in conjunction with the 50 th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-50), October 15, 2017, Boston, MA, USA.

Program Committees

ScalCom 2020	20 th International Conference on Scalable Computing and Communications (ScalCom'20). December 8-10 2020, Melbourne, Australia
CEESD 2020	5 th International Conference on Environmental Engineering and Sustainable Development (CEESD 2020). December 3-6, 2020, Xishuangbanna, China.
BigDataSE2020	14 th IEEE International Conference on Big Data Science and Engineering (IEEE BigDataSE 2020). November 10-13, 2020. Guangzhou, China.
SOTICS 2020	10 th International Conference on Social Media Technologies, Communication, and Informatics (SOTICS 2020) October 18-22, 2020, Porto, Portugal.
UPIOT 2020	2020 International Conference on Ubiquitous Power Internet of Things (UPIOT 2020). Aug. 20 - 22, 2020, Xi'an, China.
CF 2020	17 th ACM International Conference on Computing Frontiers 2020 (CF'20). May 11-13, 2020, Catania, Italy.
ICCEA 2020	International Conference on Computer Engineering and Application (ICCEA2020). March 27-29, 2020, Guangzhou, China.

CTRQ 2020	13 th International Conference on Communication Theory, Reliability, and Quality of Service (CTRQ 2020) February 23-27 2020, Lisbon, Portugal.
ScalCom 2019	19 th International Conference on Scalable Computing and Communications (ScalCom'19). August 19-23 2019, Leicester, UK
NetACT19	2 nd International Conference on Networks and Advances in Computational Technologies (NetACT19). July 23-25 2019 Trivandrum, Kerala, India
NoCArc 2018	11 th International Workshop on Network on Chip Architectures (NoCArc'18). Held in conjunction with the 51 st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-50), October 20, 2018, Fukuoka City, Japan.
NoCArc 2017	10 th International Workshop on Network on Chip Architectures (NoCArc'17). Held in conjunction with the 50 th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-50), October 15, 2017, Boston, MA, USA.

Editorial Work

Exchanges	Editor for “Exchanges: The Interdisciplinary Research Journal” (ISSN 2053-9665), a scholar-led, peer-reviewed, open access, interdisciplinary, online-only journal dedicated to the publication of high-quality work by researchers in all disciplines, managed at the University of Warwick, UK.
MICPRO	Lead Guest Editor for the Special Issue: “Adaptive and Reconfigurable Embedded Systems”, Microprocessors and Microsystems (Elsevier), 2020-2021.
NanoComNet	Guest Editor for the Special Issue: “Chip-scale Nanonetworks: Recent Trends, Emerging Technologies, Disruptive Applications”, Nano Communication Networks (Elsevier) Journal, 2020.
Non-Conventional Communications and Networks	Review Editor on the Editorial Board of “Non-Conventional Communications and Networks” (specialty section of Frontiers in Communications and Networks).

I am Reviewer Board Member of the MDPI Journal of Low Power Electronics and Applications (JLPEA), and also Reviewer Editor for Frontiers in Communications and Networks, section Non-Conventional Communications and Networks.

I served as reviewer for the following Journals: MDPI Electronics, IET Computers & Digital Techniques, Elsevier Computer Languages, Systems and Structures (COMLAN), IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), Elsevier Microprocessors and Microsystems (MICPRO), Elsevier Simulation Modelling Practice and Theory (SIMPAT), Elsevier Computers and Electrical Engineering (COMPELECENG),

Elsevier Journal of Computer and System Sciences (JCSS), MDPI Journal of Low Power Electronics and Applications (JLPEA), Elsevier Nano Communication Networks (NANOCOMNET), IEEE ACCESS, ACM Journal on Emerging Technologies in Computing Systems (JETC), and Elsevier Journal of Systems Architecture (JSA).

Publications

Journals

1. S. Mnejja, Y. Aydi, M. Abid, S. Monteleone, V. Catania, M. Palesi, D. Patti. Delta Multi-Stage Interconnection Networks for Scalable Wireless On-Chip Communication. *Electronics*, 9(6), 913, MDPI 2020
2. G. Ascia, V. Catania, S. Monteleone, M. Palesi, D. Patti, J. Jose, and V. M. Salerno. Exploiting Data Resilience in Wireless Network-on-chip Architectures. *Journal on Emerging Technologies in Computing Systems (JETC)*, 16(2), 1-27, ACM 2020.
3. V. Catania, S. Monteleone, M. Palesi, and D. Patti. Impact of Users' Beliefs in Text-Based Linguistic Interaction. *IEEE Access*, 8, 46861-46867, IEEE 2020.
4. V. Catania, G. La Delfa, G. La Torre, S. Monteleone, D. Patti, and D. Ventura. GOOSE: Goal Oriented Orchestration for Smart Environments. *International Journal of Ad Hoc and Ubiquitous Computing*, 32(3), 159-170, Inderscience, 2019.
5. V. Catania, A. Mineo, S. Monteleone, M. Palesi, and D. Patti. Improving energy efficiency in wireless network-on-chip architectures. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 14(1):9, ACM 2017.
6. V. Catania, G. La Torre, S. Monteleone, D. Panno, and D. Patti. User-generated services composition in smart multi-user environments. *Journal of Sensor and Actuator Networks*, 6(3):20, MDPI 2017.
7. V. Catania, A. Mineo, S. Monteleone, M. Palesi, and D. Patti. Cycle-accurate Network on Chip Simulation with Noxim. *ACM Transactions on Modeling and Computer Simulation (TOMACS)*, 27(1):4, ACM 2016.
8. G. C. La Delfa, S. Monteleone, V. Catania, J. F. De Paz, and J. Bajo. Performance analysis of visual markers for indoor navigation systems. *Frontiers of Information Technology & Electronic Engineering*, 17(8):730–740, Frontiers 2016.
9. V. Catania, A. Mineo, S. Monteleone, and D. Patti. Distributed Topology Discovery in Self-Assembled Nano Network-on-Chip. *Computers & Electrical Engineering*, 40(8):292–306, Elsevier 2014.

Chapter in Books

1. V. Catania, S. Monteleone, M. Palesi, and D. Patti. The Web As A Platform For Experimental Human-Computer Linguistic Interaction. In *Machine Vision and Human-Machine Interface Technologies, Applications and Challenges*, Chapter 2, Nova Publishers, ISBN: 978-1-63484-052-1.

Conferences

1. G. Ascia, V. Catania, J. Jose, S. Monteleone, M. Palesi, and D. Patti. Improving Inference Latency and Energy of Network-on-Chip based Convolutional Neural Networks through Weights Compression. Heterogeneity in Computing Workshop held in conjunction with the 34th IEEE International Parallel & Distributed Processing Symposium (IPDPS), May 18-22, 2020, New Orleans, Louisiana, USA. Held virtually during the week of the conference.
2. H. Lahdhiri, M. Palesi, S. Monteleone, D. Patti, G. Ascia, J. Lorandel, E. Bourdel, and V. Catania. DNNZip: Selective Layers Compression Technique in Deep Neural Network Accelerators. Euromicro Conference on Digital System Design, Euromicro DSD'2020, August 26-28, 2020, Portorož, Slovenia. Held virtually during the week of the conference.
3. J. Lorandel, H. Lahdhiri, E. Bourdel, S. Monteleone, and M. Palesi. Efficient Compression Technique for NoC-based Deep Neural Network Accelerators. Euromicro Conference on Digital System Design, Euromicro DSD'2020, August 26-28, 2020, Portorož, Slovenia. Held virtually during the week of the conference.
4. S. Mnejja, Y. Aydi, M. Abid, S. Monteleone, M. Palesi, D. Patti. Implementing On-Chip Wireless Communication in Multi-stage Interconnection NoCs. In Proceedings of the 34th International Conference on Advanced Information Networking and Applications, Caserta, Italy, (pp. 533-546). Springer, Cham 2020.
5. G. Ascia, V. Catania, S. Monteleone, M. Palesi, D. Patti and J. Jose. Analyzing networks-on-chip based deep neural networks. In Proceedings of the 6th International Conference on Internet of Things: Systems, Management and Security, IOTSMS 2019, Granada, Spain, pp. 227-234. IEEE 2019
6. G. Ascia, V. Catania, S. Monteleone, M. Palesi, D. Patti and J. Jose. Analyzing networks-on-chip based deep neural networks. In Proceedings of the 13th IEEE/ACM International Symposium on Networks-on-Chip, NOCS 2019, New York, USA.
7. G. Ascia, V. Catania, S. Monteleone, M. Palesi, D. Patti and J. Jose. Approximate Wireless Networks-on-Chip. In 33rd Conference on Design of Circuits and Integrated Systems, DCIS 2018, Lyon, France, 2018.
8. G. Ascia, V. Catania, S. Monteleone, M. Palesi, D. Patti and J. Jose. Improving energy consumption of NoC based architectures through approximate communication. In 7th Mediterranean Conference on Embedded Computing (MECO), Budva, 2018, pp. 1-4. IEEE, 2018.
9. V. Catania, S. Monteleone, M. Palesi, and D. Patti. Packetization of Shared-Memory Traces for Message Passing Oriented NoC Simulation. In: Yokota R., Weiland M., Keyes D., Trinitis C. (eds) High Performance Computing. ISC High Performance 2018. Lecture Notes in Computer Science, vol 10876. Springer, Cham, 2018.
10. S. M. Biondi, V. Catania, S. Monteleone, M. Palesi and D. Patti. smARTWorks: A multi-sided context-aware platform for the smart museum. In Proceedings of the 8th International Joint Conference on Pervasive and Embedded Computing and Communication Systems - Volume 1: PECCS, pages 103-109.

11. S. M. Biondi, V. Catania, S. Monteleone, and C. Polito. Bus as a sensor: A mobile sensor nodes network for the air quality monitoring. In *Wireless and Mobile Computing, Networking and Communications (WiMob)*, pages 272–277. IEEE, 2017.
12. S. M. Biondi, S. Monteleone, G. La Torre, and V. Catania. A context-aware smart parking system. In *Signal-Image Technology & Internet-Based Systems (SITIS), 2016 12th International Conference on*, pages 450–454. IEEE, 2016.
13. G. La Torre, S. Monteleone, M. Cavallo, V. D’Amico, and V. Catania. A Context-Aware Solution to Improve Web Service Discovery and User-Service Interaction. In *Ubiquitous Intelligence & Computing, Advanced and Trusted Computing, Scalable Computing and Communications, Cloud and Big Data Computing, Internet of People, and Smart World Congress (UIC/ATC/ScalCom/CBDCom/IoP/SmartWorld), 2016 Intl IEEE Conferences*, pages 180–187. IEEE, 2016.
14. G. Ascia, V. Catania, R. Di Natale, A. Fornaia, M. Mongiovi, S. Monteleone, G. Pappalardo, and E. Tramontana. Making android apps data-leak-safe by data flow analysis and code injection. In *2016 IEEE 25th International Conference on Enabling Technologies: Infrastructure for Collaborative Enterprises (WETICE)*, pages 205–210. IEEE, 2016.
15. V. Catania, A. Mineo, S. Monteleone, M. Palesi, and D. Patti. Energy efficient transceiver in wireless Network on Chip architectures. In *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1321–1326. IEEE, 2016.
16. V. Catania, A. Mineo, S. Monteleone, M. Palesi, and D. Patti. Improving the energy efficiency of wireless Network on Chip architectures through online selective buffers and receivers shutdown. In *2016 13th IEEE Annual Consumer Communications & Networking Conference (CCNC)*, pages 668–673. IEEE, 2016.
17. V. Catania, G. La Torre, S. Monteleone, D. Panno, and D. Patti. User-Generated Services: Policy management and access control in a cross-domain environment. In *2015 International Wireless Communications and Mobile Computing Conference (IWCMC)*, pages 668–673. IEEE, 2015.
18. V. Catania, A. Mineo, S. Monteleone, M. Palesi, and D. Patti. Noxim: An open, extensible and cycle-accurate Network on Chip simulator. In *2015 IEEE 26th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 162–163. IEEE, 2015.
19. D. Ventura, S. Monteleone, G. La Torre, G. C. La Delfa, and V. Catania. Smart EDIFICE - Smart EveryDay interoperating future devICES. In *Collaboration Technologies and Systems (CTS), 2015 International Conference on*, pages 19–26. IEEE, 2015.
20. G. C. La Delfa, V. Catania, S. Monteleone, J. F. De Paz, and J. Bajo. Computer Vision Based Indoor Navigation: A Visual Markers Evaluation. In *Ambient Intelligence-Software and Applications*, pages 165–173. Springer International Publishing, 2015.
21. D. Patti, A. Mineo, S. Monteleone, and V. Catania. Topology Discovery in Deadlock Free Self-assembled DNA Networks. In *Modern Trends and Techniques in Computer Science*, pages 301–311. Springer International Publishing, 2014.
22. V. Catania, A. Mineo, S. Monteleone, and D. Patti. A low-resource and scalable strategy

for segment partitioning of many-core nano networks. In Proceedings of International Workshop on Manycore Embedded Systems, page 17. ACM, 2014.

23. V. Catania, A. Mineo, S. Monteleone, and D. Patti. A first effort for a distributed segment-based approach on self-assembled nano networks. In Proceedings of the Sixth International Workshop on Network on Chip Architectures, pages 59–64. ACM, 2013.
24. V. Arena, V. Catania, G. La Torre, S. Monteleone, and F. Ricciato. SecureDroid: An Android Security Framework Extension for Context-Aware Policy Enforcement. In Privacy and Security in Mobile Systems (PRISMS), 2013 International Conference on. IEEE, 2013.
25. V. Catania, G. La Torre, S. Monteleone, D. Patti, S. Vercelli, and F. Ricciato. A novel approach to Web of Things: M2M and enhanced Javascript technologies. In Green Computing and Communications (GreenCom), 2012 IEEE International Conference on, pages 726–730. IEEE, 2012.
26. J. Lyle, S. Monteleone, S. Faily, D. Patti, and F. Ricciato. Cross-platform access control for mobile web applications. In Policies for Distributed Systems and Networks (POLICY), 2012 IEEE International Symposium on, pages 37–44. IEEE, 2012.
27. S. Cavalieri, G. Cutuli, and S. Monteleone. Evaluating impact of security on OPC UA performance. In Human System Interactions (HSI), 2010 3rd Conference on, pages 687–694. IEEE, 2010.

Conferences (in press)

1. Improving Inference Latency and Energy of DNNs through Wireless Enabled Multi-Chip-Module-based Architectures and Model Parameters Compression. 14th IEEE/ACM International Symposium on Networks-on-Chip, NOCS 2020, September 24 – 25, 2020. Held virtually during the week of the conference.

Salvatore Monteleone
