High-Throughput Hard Decision LDPC Decoder Architectures Using Imprecise Units

Oana Boncalo

<u>Motivation</u>: Future telecommunication standards will enable very high throughputs, in the range of tens to hundreds of Gbps. Furthermore, we the advent of pico and femto cells, the transmission/receive power consumption will be similar to the one used in the digital processing of the transmitted data packets. Therefore, simpler and less complex error correction decoding techniques are required. Although hard decision LDPC decoding has less error correction capability with respect to the soft decision counterparts, its significantly lower complexity make them suitable candidates for very high throughput, low power applications, such as the future telecom standards. In this project, we will investigate methods for throughput increase of a wide range of hard decision LDPC decoding algorithms, such as Gallagher B, two-bit bit flipping [1], or Gradient Descent Bit Flipping (GDBF)[2], in order to achieve rates of tens to hundreds of Gbps.

<u>Objectives and Methodology</u>: In this project, we will investigate methods and algorithms modifications for throughput increase of hard-decision LDPC decoding architectures. The technical contributions will focus on three directions:

- Methods for low latency computations of the global maximum in GDBF using imprecise arithmetic units: the main challenge from the hardware perspective in GDBF algorithms is represented by computation of the global minimum/maximum at variable node level [2]; this computation of the global minimum/maximum represents a major component in the overall cost of the GDBF decoders, as well as the main frequency limiting factor; we will investigate imprecise methods to greatly reduce the complexity of this component, while having only limited decoding performance degradation [4];
- Layered and iteration based un-rolling of hard decision LDPC decoding for increased throughput – iteration based un-rolling has been applied for Min-Sum based decoders for throughput increase [3]; we will investigate these types of methods for hard-decision decoders in order to achieve several hundreds of Gbps data rates
- 3. Imprecise early termination criterion for hard decision LDPC decoding early termination may lead to significant power reduction, as well as throughput increase in decoding; however, the circuitry implementing early termination may add significant cost overhead; we will investigate imprecise methods which will result in significant cost reduction [5]

<u>Contribution to France-Romania Scientific Collaboration</u>: In addition to technical contributions, this project will greatly contribute to continuing the fruitful collaboration between the University of Cergy Pontoise and University Politehnica Timisoara, which includes the continuation of the research activities on the Romania-France (UEFISCDI-ANR Blanc) DIAMOND project, where both ENSEA-ETIS and University Politehnica Timisoara are project partners. The collaboration between the two universities has resulted in several joint publications between the two research groups, as well as a future patent application on the termination criterion for layered LDPC decoders.

References

- D. V. Nguyen, B. Vasic "Two-Bit Bit Flipping Algorithms for LDPC Codes and Collective Error Correction" IEEE Trans. On Communication, Vol. 62, Issue 4, 2014
- [2] K. Le, D. Declercq, F. Ghaffari, C. Spagnol, E. Popovici, B. Vasic, P. Ivanis "Efficient realization of probabilistic gradient descent bit flipping decoders" Proc. 2015 IEEE Int. Symp. On Circuits and Systems (ISCAS), 2015
- P. Schlafer, N. Wehn, M. Alles, T. Leighnik-Éden " A New Dimension of Parallelism in Ultra High Throughput LDPC Decoders" Proc. 2013IEEE Workshop on Signal Processing Systems, 2013
- [4] O. Boncalo, A. Amaricai, V. Savin, D. Declercq, F. Ghaffari "Check node unit for LDPC decoders based on one-hot data representation of messages" Electronics Letters, Vol. 51, Issue 12, 2015
- [5] A. Hera, O. Boncalo, C.E. Gavriliu, A. Amaricai, V. Savin, D. Declercq, F. Ghaffari "Analysis and implementation of on-the-fly stopping criteria for layered QC LDPC decoders" Proc. 2015 22nd Int. Conf. on Mixed Design of Integrated Circuits and Systems (MIXDES), 2015