Stochastic Resonance in Error Correction Coding and Machine Learning Algorithms for Data Storage

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Targeted Need: It is widely recognized that sustainable progress for data storage can be only achieved through highly energy-efficient components. The main obstacle is these low-powered components are inherently noisy and unreliable. **The objective of the proposed research is to overcome this unreliability by developing a comprehensive theoretical framework and hardware based on Error Correcting Codes (ECC) that embrace noisy components to noisy brain-inspired computing**. More specifically, we will target the design of ECCs and encoding–decoding and machine learning algorithms to provide reliable error protection even if the encoders and decoders themselves operate on unreliable hardware. This non-Von Neumann information theory approach addresses the needs for data storage and processing.

Approach: The methodology relies on our recent discovery of stochastic resonance phenomena in iterative decoders for low-density parity check (LDPC) codes [1,2,3,4,5]. The unreliability and noise in logic gates comprising a decoder are not necessarily detrimental, and the main idea is to use the positive effect of errors in logic gates in order to correct errors in memory data storage elements. This effect is illustrated in Figure 1 for a Gallager B decoder, with the lowest probability of error—and best performance—obtained for a noisy decoder in which the logic gate error probability is relatively high. This novelty recognizes that the decoder—essentially an iterative minimization of the Bethe free energy on the code graph—can get trapped in local minima, and random perturbations help the decoder to escape from these minima and converge to a correct codeword. Crucially, such useful random perturbations require neither additional hardware nor energy, as they are built into noisy hardware itself. This opens fundamentally new avenues for designing energy efficient storage systems.

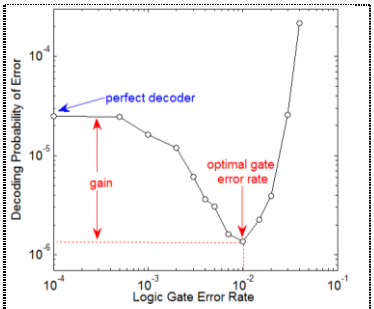

Figure 1 Stochastic resonance in Gallager B decoding algorithm. The memory element error rate is 0.006.

Objective and Results: In NSF funded projects CCF-0634969 and CCF-0963726 we developed the knowledge base and intuition that evolved to the paradigm-changing idea underpinning this proposal. Based on this novel theory, advanced decoders will be designed and their performance characterized. To optimize algorithms and accelerate measurements, we will develop an FPGA environment with appropriate error, noise, and energy models for the target technologies such as Spin Transfer Torque Random Access and 3D NAND Flash. We will rely for that environment on the recent plateform bought in ETIS laboratory: ProFPGA Quad System based on Ultra Scale XCVU440: http://www.prodesign-europe.com/proFPGA_Products_XCVU440_FM.html. This platform is capable of capturing error rates of 10^{-10} and operating with code lengths of up to 4000 bits—both are required to fully demonstrate applicability to practical storage systems, and are key challenges for the

project. Our goal at the end of the project is to make low-power, decoder architectures that improve error probability by two orders of magnitude, and thus accomplish correct logic operation at the target low energy budgets under which the current standard designs are completely inoperable. We will uncover the fundamental underlying features of decoding algorithms that can leverage and benefit from randomness- a phenomenon similar to genetic algorithms used in optimization. This will lead to methods for optimizing decoder architectures, which we will investigate next. The proposed paradigm shift involves relying on bit-flipping and message passing decoders. Routability is the primary barrier for the FPGA based parallel decoder architectures as the routing resource demand shows polynomial growth rate as a function of codeword length, number of processing elements and two-terminal connections. We propose to design and implement a model-based approach for evaluating the impact of architectural design choices on performance and identifying the parallelization strategy that result with sublinear growth rate. The proposed hardware and software optimization environment will facilitate the way decoder algorithms can be re-expressed and customized to the performance requirements of the application through parallel constructs. We will then complete a hardware simulation environment to perform large-scale tests on noise/error scenarios and design the decoders.

Visit Request: To supporting the proposed activity, a support for two visits in duration not longer than **two months** in total is requested. The first visit will be approximately middle **November 2017**, and the second in **June 2018**. Professor Vasić is a 2012 IEEE Fellow, Fulbright Scholar, da Vinci Fellow and past Chair of the IEEE Data Storage Technical Committee. He is world-recognized expert in coding theory and information storage.

References:

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[2] **Fakhreddine Ghaffari**, Ali Akoglu, **Bane Vasic** and David Declercq, "Multi-mode Low-latency Software-defined Error Correction for Data Centers", invited paper, *2017 26th International Conference on Computer Communication and Networks (ICCCN)*, Vancouver, Canada, August 2017.

[3] Khoa Le, **Fakhreddine Ghaffari**, David Declercq, **Bane Vasic** and Chris Winstead "A Novel High-Throughput, Low-Complexity Bit-Flipping Decoder for LDPC Codes" in International Conference on Advanced Technologies for Communications, (ATC 2017), October 18- 20, Quynhon, Vietnam.

[4] Khoa Le, **Fakhreddine Ghaffari**, David Declercq, **Bane Vasic**, "Hardware Optimization of the Perturbation for Probabilistic Gradient Descent Bit Flipping Decoders" in Circuits and Systems (ISCAS 2017), IEEE International Symposium on, **Best Student Papers (Honorable Mention),** 28-31 May 2017

[5] Burak Unal, **Fakhreddine Ghaffari**, Ali Akoglu, David Declercq and **Bane Vasic** "Analysis and Implementation of Resource Efficient Probabilistic Gallager B LDPC Decoder", in New Circuits and Systems Conference (NEWCAS), 2017 IEEE 15th International, 25-28 June 2017, Strasbourg, France.